REMARKS

The Office Action mailed December 21, 2000, has been received and reviewed. Claims 1-101 are currently pending in the application. Claims 1-16 and 34-49, which have been withdrawn from consideration as being drawn to a nonelected invention, have been canceled without prejudice or disclaimer. Claim 73 has also been canceled without prejudice or disclaimer. Claims 17-33 and 50-101 stand rejected. It is respectfully submitted that the amendments presented herein are merely for the purpose of clarity, and that these amendments have been made without prejudice or disclaimer to the previously recited subject matter. Reconsideration of the application is respectfully requested in view of the amendments and remarks presented herein.

Rejections Under 35 U.S.C. § 112, Second Paragraph

Claims 83 and 89 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 83 and 89 have each been amended to recite that selected regions of the photoresist are exposed, as, for purposes of examination, was properly presumed in the outstanding Office Action. It is, therefore, respectfully requested that the rejections of claims 83 and 89 under the second paragraph of section 112 be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Fischer in View of Sandhu

Claims 17 and 19-33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,185,291 to Fischer et al. (hereinafter "Fischer") in view of U.S. Patent 5,231,056 to Sandhu (hereinafter "Sandhu").

Fischer teaches a fuse for use in a semiconductor device structure, as well as a process for fabricating the fuse. The fuse of Fischer, which is disposed over an insulative structure, such as a field oxide region, includes a first conductive layer and a second conductive layer. The first conductive layer, which may be formed from aluminum or tungsten, includes two spaced apart end regions. The second conductive layer of the fuse is preferably formed from the same material as the first layer, but may also be formed from polysilicon. End portions of the second conductive layer overlie the spaced apart regions of the first conductive layer, while the central portion of the second conductive layer is located in substantially the same plane as the first conductive layer and between the spaced apart portions of the first conductive layer.

Fischer teaches that the fuse may be fabricated by forming a first layer of conductive material over an insulative structure, patterning a "window" in the first layer of conductive material to expose a portion of the underlying insulative structure, forming a second layer of conductive material over the first layer and within the window, and patterning the "combined" first and second layers to form the fuse.

The fuse of Fischer is designed to rupture upon exposure of the central region of the second conductive layer to a laser beam.

Sandhu teaches a chemical vapor deposition (CVD) method for forming tungsten silicide. Sandhu suggests that the method may be useful in transistor gate fabrication processes for forming a polycide (i.e., polysilicon-tungsten silicide) gate structure.

Independent claim 17, as amended and presented herein, recites a method for fabricating a fuse. The method of claim 17 includes, among other things, patterning a layer of conductive material to define at least two individual, spaced apart regions, between which an underlying insulative structure is exposed. The method of claim 17 also includes disposing a layer of metal silicide over and between the two regions of conductive material.

First, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Fischer and Sandhu in the manner that is suggested in the outstanding Office Action. Specifically, neither Fischer, Sandhu, nor the teachings that were generally available to those of ordinary skill in the art before the filing date of the referenced application would provide any motivation to the ordinarily skilled artisan to modify the teachings of Fischer by forming a second conductive layer from a metal silicide, let alone by the process disclosed in Sandhu.

It is further submitted that the asserted motivation provided in the outstanding Office Action – that metal silicides provide "low bulk resistance and low stress"– is not sufficient to have motivated one of ordinary skill in the art to substitute the use of tungsten silicide for aluminum or tungsten to form the second conductive layer of the fuse taught in Fischer, as aluminum and tungsten have even lower bulk resistances than that of tungsten silicide formed in accordance with the method of Sandhu. It appears that any such motivation could only have been based on hindsight provided by the specification or claims of the referenced application.

Second, even if one of ordinary skill in the art would have been motivated to combine the teachings of Fischer and Sandhu in the manner that has been set forth in the outstanding Office Action, it is respectfully submitted that neither Fischer nor Sandhu, taken alone or in combination, teaches each and every element of claim 17. By way of contrast with amended independent claim 17, neither Fischer nor Sandhu, taken alone or in combination, teaches a fuse fabrication method that includes patterning a layer of conductive material to form at least two individual, spaced apart regions with an underlying insulative structure exposed therethrough. Rather, Fischer merely teaches forming a window through the first layer of conductive material. When the second conductive layer is formed, the insulative structure is no longer exposed through the window. The fuse itself is not formed until after the second layer of conductive material has been formed. Sandhu neither teaches or suggests a fuse fabrication method.

In addition, both Fischer and Sandhu lack any teaching or suggestion of disposing and patterning a layer of metal silicide to define terminal regions and a central region of a fuse, as is recited in amended claim 17. Rather, Fischer only teaches that such structures may be formed from aluminum, tungsten, or polysilicon. Sandhu does not teach or suggest that tungsten silicide

formed in accordance with the method thereof may be used to form either a terminal region or a central region of a fuse.

Claims 19-33 are each allowable, among other reasons, as depending either directly or indirectly from claim 17, which should be allowed.

In view of the foregoing, it is respectfully requested that the Office withdraw the rejections of claims 17 and 19-33 under 35 U.S.C. § 103(a).

Fischer in View of Sandhu and Further in View of Szluk

Claim 18 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Fischer in view of Sandhu, as applied to claim 17 above, and further in view of U.S. Patent 4,647,340 to Szluk et al. (hereinafter "Szluk").

The teachings of Fischer and Sandhu have been summarized above.

Szluk teaches a so-called "antifuse" and a method for fabricating the antifuse. The antifuse of Szluk includes a conductively doped region of a semiconductor substrate and a conductive element, which includes a polysilicon layer and a tungsten layer, that extends close to the conductively doped region, but is separated therefrom by way of a thin dielectric structure. A contact structure communicates with the conductively doped region of the substrate. Upon applying a sufficient voltage to the contact structure, the thin dielectric structure ruptures, facilitating electrical communication between the conductively doped region of and the conductive element and enabling the antifuse to conduct an electrical current thereacross.

The antifuse of Szluk may be fabricated concurrently with the fabrication of a transistor gate structure. Once the substrate is conductively doped, the thin dielectric layer is formed and patterned. A polysilicon layer is then formed and patterned, as is a tungsten layer that overlies the polysilicon layer.

Claim 18 is allowable, among other reasons, as depending from claim 17, which should be allowed.

It is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Szluk with those of either Fischer or Sandhu. Specifically, Szluk does not provide the motivation that is missing from both Fischer and Sandhu

to fabricate the second conductive layer of the fuse taught in Fischer from a layer of metal silicide.

Moreover, Szluk does not teach or suggest that the polysilicon layer is patterned to form at least two individual, spaced apart regions. Nor does Szluk teach or suggest that the tungsten layer or, for that matter, a metal silicide layer, is disposed over or between the at least two regions of polysilicon or that the tungsten layer is patterned to form a terminal region or a central region of a fuse. As neither Fischer nor Sandhu teach or suggest these elements either, it is respectfully submitted that, under 35 U.S.C. § 103(a), claim 18 is allowable over the combination of these references.

For these reasons, it is respectfully requested that the rejection of claim 18 under 35 U.S.C. § 103(a) be withdrawn.

Fischer in View of Sandhu and Further in View of Szluk

Claims 50, 51, and 55-68 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fischer in view of Sandhu, and further in view of Szluk.

The teachings of each of these references have been summarized previously herein.

For the same reasons provided above with respect to claim 18, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Fischer, Sandhu, and Szluk in the manner that has been suggested in the outstanding Office Action.

Moreover, it is respectfully submitted that Fischer, Sandhu, and Szluk, taken either alone or in combination, do not teach or suggest each and every element of claims 50, 51, and 55-68.

Independent claim 50, as amended and presented herein, recites a method for fabricating a fuse that includes, among other things, fabricating individual, spaced apart regions comprising polysilicon on an insulative structure and fabricating a fuse comprising a metal silicide. The fabricated fuse includes a central region located adjacent the insulative structure and between the spaced apart regions, as well as at least two terminal regions on opposite ends of the central region and adjacent the spaced apart regions that comprise polysilicon.

None of Fischer, Sandhu, or Szluk teaches or suggests a fuse fabrication method that includes fabricating spaced apart regions comprising polysilicon on an insulative structure.

Rather, Fischer merely teaches that polysilicon may be used to form the second layer of the fuse thereof. Moreover, none of these references teaches or suggests a fuse fabrication method that includes forming from a metal silicide a fuse that includes a central region and at least two terminals, with the at least two terminals being located over spaced apart regions comprising polysilicon. For these reasons, it is respectfully submitted that, under 35 U.S.C. § 103(a) amended independent claim 50 is allowable over Fischer, Sandhu, and Szluk, taken alone or in combination.

Each of claims 51 and 55-68 is allowable, among other reasons, as depending either directly or indirectly from claim 50, which should be allowed.

For these reasons, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 50, 51, and 55-68 be withdrawn.

Fischer in View of Sandhu and Further in View of Szluk and Degelormo

Claims 52-54, 69, and 70 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fischer in view of Sandhu, further in view of Szluk, as applied to claims 50 and 51 above, and further in view of U.S. Patent 5,242,859 to Degelormo et al. (hereinafter "Degelormo").

Degelormo merely teaches a chemical vapor deposition method for forming layers of conductively doped polysilicon. Degelormo includes no teaching or suggestion that the CVD process thereof may be used to fabricate any part of a fuse or structures associated directly with a fuse, let alone individual, spaced apart regions comprising polysilicon over an insulative structure.

Claims 52-54, 69, and 70 are each allowable, among other reasons, as depending either directly or indirectly from claim 50, which should be allowed.

Therefore, it is respectfully requested that the Office withdraw the rejection of claims 52-54, 69, and 70 under 35 U.S.C. § 103(a).

Fischer in View of Szluk and Bohr

Claims 71, 80-86, 88-92, and 101 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fischer in view of Szluk, and further in view of U.S. Patent 5,969,404 to Bohr et al. (hereinafter "Bohr").

The teachings of Fischer and Szluk have been summarized previously herein.

Bohr teaches a fuse that includes a polysilicon layer and an overlying metal silicide layer, as well as a method for fabricating the fuse. Both the polysilicon layer and the metal silicide layer extend the complete length of the fuse. The fuse is "blown" when a sufficient voltage is applied to the metal silicide layer to cause the metal silicide to agglomerate, rendering the metal silicide layer discontinuous at some point along the length of the fuse. As a result of being blown, an electrical current must traverse the fuse through the polysilicon layer, which has a greater resistance than the metal silicide layer.

It is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Fischer, Szluk, and Bohr in the manner that has been suggested in the outstanding Office Action. Fischer, Szluk, and Bohr teach three very different types of fuses. Fischer teaches a fuse that is programmed with a laser rather than with an electrical current. Szluk teaches an antifuse that includes a dielectric structure that is blown when a sufficient voltage is applied to the antifuse, causing the antifuse to more readily convey an electrical current. Bohr teaches a fuse that conveys an electrical current until it is blown by applying a sufficient voltage thereacross, increasing the fuse's resistance to the flow of an electrical current thereacross. As these references teach different types of fuses that operate in entirely different manners, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to apply the fabrication processes of any of these fuses to the fabrication processes of any of the others of these fuses in a way that would have rendered obvious the presently claimed method. It is further submitted that any motivation to combine the teachings of Fischer, Szluk, and Bohr in the manner that has been set forth in the outstanding Office Action could only have been gleaned from the hindsight provided by the specification and claims of the referenced application.

Second, it is respectfully submitted that Bohr teaches away from the method recited in amended independent claim 71. Specifically, Bohr teaches a fuse that includes a polysilicon layer that extends across the entire length thereof, as well as a method for fabricating such a polysilicon layer, whereas amended independent claim 71 recites a method that includes patterning regions of a layer of polysilicon to form individual, spaced apart regions of polysilicon.

Third, it is respectfully submitted that Fischer, Szluk, and Bohr, taken either alone or in combination, do not teach or suggest each and every element of amended independent claim 71. Specifically, none of Fischer, Szluk, or Bohr teaches or suggests a fuse fabrication method that includes "patterning at least regions of said layer of polysilicon disposed over at least one field oxide region of said field oxide regions to define at least two individual, spaced apart regions from said polysilicon over said at least one field oxide region with a portion of said at least one field oxide region being exposed therebetween" and "disposing a layer of metal silicide on said layer of polysilicon and into contact with said [exposed] portion of said at least one field oxide region". Therefore, under 35 U.S.C. § 103(a), claim 71, as amended and presented herein, is allowable over Fischer, Szluk, and Bohr.

Claims 80-86, 88-92, and 101 are each allowable, among other reasons, as depending either directly or indirectly from claim 71, which should be allowed.

For the foregoing reasons, it is respectfully requested that the Office withdraw the 35 U.S.C. § 103(a) rejections of claims 71, 80-86, 88-92, and 101.

Szluk in View of Bohr and Further in View of Degelormo

Claim 72 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Szluk in view of Bohr, and further in view of Degelormo.

Claim 72 is allowable, among other reasons, as depending from claim 71, which should be allowed.

Szluk in View of Bohr and Further in View of Fischer

Claims 73-79 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Szluk in view of Bohr, as applied to claim 71 above, and further in view of Fischer.

Claim 73 has been canceled without prejudice or disclaimer, rendering the rejection of this claim moot.

Each of claims 74-79 is allowable, among other reasons, as depending either directly or indirectly from claim 71, which should be allowed.

Szluk in View of Bohr and Further in View of Sandhu

Claim 87 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Szluk in view of Bohr, as applied to claim 71 above, and further in view of Sandhu.

The teachings of Szluk, Bohr, and Sandhu have been summarized previously herein. Again, Sandhu merely teaches a process by which tungsten silicide may be formed.

Claim 87 is allowable as depending from claim 71, which should be allowed, for the same reasons provided above with respect to claim 71, and, further, because Sandhu does not provide the motivation that would be necessary to combine the teachings of Szluk and Bohr.

Szluk in View of Bohr and Further in View of Ukeda

Claims 93-100 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Szluk in view of Bohr, as applied to claim 71 above, and further in view of U.S. Patent 6,069,055 to Ukeda et al. (hereinafter "Ukeda").

Ukeda teaches a dry etch process for anisotropically removing exposed regions of a polysilicon layer through a metal silicide layer. Ukeda does not teach or suggest that the process disclosed therein may be used in fabricating a fuse.

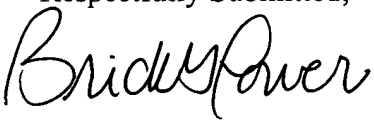
Claims 93-100 are each allowable, among other reasons, as depending directly or indirectly from claim 71, which should be allowed. Claims 93-100 are also allowable since Ukeda does not supply the motivation that would be required to combine the teachings of Szluk and Bohr.

Accordingly, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 93-100 be withdrawn.

CONCLUSION

It is respectfully submitted that each of claims 17-33, 50-72, and 74-101 is in condition for allowance. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the referenced application has been passed for issuance. If any issues preventing the allowance of any of claims 17-33, 50-72, and 74-101 remain that might be resolved by way of a telephone conference, the Office is respectfully invited to contact the undersigned.

Respectfully Submitted,



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Enclosure: VERSION WITH MARKINGS TO SHOW CHANGES MADE

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

17. (Twice amended) A method of fabricating a fuse upon a semiconductor device, comprising:

disposing a layer of conductive material over an insulative structure of the semiconductor device;

patterning said layer of conductive material to define at least two individual, spaced apart regions of conductive material [through] between which said insulative structure is exposed;

disposing a layer of metal silicide over the semiconductor device, including adjacent to said at least two regions and to said insulative structure exposed between said at least two regions; and

patterning said layer of metal silicide so as to define at least two terminal regions of the fuse, each of which is in contact with a corresponding one of said at least two regions of conductive material, and a central region disposed between said at least two terminal regions and in contact with said insulative structure.

50. (Twice amended) A method of fabricating a fuse, comprising:

fabricating individual, spaced apart regions comprising polysilicon on an insulative structure of a semiconductor device; and

fabricating a fuse comprising a metal silicide, including a central region disposed adjacent the insulative structure and between said spaced apart regions and at least two terminal regions disposed on opposite ends of the central region and adjacent said spaced apart regions.

71. (Twice amended) A method of substantially simultaneously fabricating a gate and a fuse on a semiconductor substrate, comprising:

disposing a layer of insulative material over at least an exposed region of the semiconductor substrate;

disposing a layer of polysilicon over the semiconductor substrate, including over said layer of insulative material and over field oxide regions disposed on the semiconductor substrate;

patterning at least regions of said layer of polysilicon disposed over at least one field oxide region of said field oxide regions to define at least two individual, spaced apart regions from said polysilicon over said at least one field oxide region with a portion of said at least one field oxide region being exposed therebetween;

disposing a layer of metal silicide on said layer of polysilicon and into contact with said portion of said at least one field oxide region;

patterning at least said layer of metal silicide to define the fuse and the gate therefrom.

74. (Amended) The method of claim [73] 71, wherein said defining the fuse comprises defining a central region disposed adjacent and substantially between said at least two spaced apart regions and defining at least two terminal regions, each terminal region continuous with an end of said central region and disposed adjacent one of said at least two spaced apart regions.

75. (Amended) The method of claim [73] 71, wherein said defining said at least two spaced apart regions comprises disposing a mask over said layer of polysilicon and removing selected regions of said layer of polysilicon through said mask.

83. (Amended) The method of claim 82, wherein said disposing said mask comprises disposing photoresist over said layer of polysilicon, exposing selected regions of said [layer of polysilicon] photoresist, and developing said selected regions.

89. (Amended) The method of claim 88, wherein said disposing said mask comprises disposing photoresist over said layer of metal silicide, exposing selected regions of said [layer of metal silicide] photoresist, and developing said selected regions.